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System-on-a-Chip Development for Small Satellite Onboard Data Handling

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This paper presents research work aimed at miniaturization of the onboard data handling system of a small satellite. A mixed-mode application-specific integrated circuit that represents a single chip implementation of an onboard command and data handling subsystem for a low-cost small satellite is outlined. A system-on-a-chip design of an onboard computer is proposed, which is based on integration of soft intellectual property cores. A downsized onboard computer implementation on a single programmable logic chip and a low-cost communication system are described. Details about the design and integration of a mathematical floating-point co-processor core, based on the CORDIC algorithm, are given. Reconfigurability aspects are discussed.

I. Introduction

The knock-on effects of the enduring trend towards ever smaller electronic components have already brought on significant size reductions in aerospace systems. Future advances are set to pave the way for a new class of science and exploration missions. Satellites are generally classified by weight, with standard ones weighing a ton or more, small satellites coming in between 100 kg and a ton, and microsatellites are considered to be those that fall between 10 and 100 kg. The up-and-coming new wave of smaller satellites currently in the pipeline are so-called nanosatellites, ranging from 10 kg down to 1 kg, and picosatellites that weigh in at less than 1 kg. The smallest category envisioned is the femtosatellites at less than one-tenth of a kilogram. A newly coined term "satellite-on-a-chip" is used for a highly integrated femtosatellite implemented on a single chip that can be mass-produced.[1] The Surrey Space Centre (SSC) in Guildford, UK, has a research program, codenamed ChipSat, which aims to apply advanced micro- and nanotechnologies to small satellite design. The long-term goal of the ChipSat program is to build a satellite-on-a-chip device for use in multi-node "virtual satellite" missions. Current research activities are focused on applying a system-on-a-chip (SoC) approach to miniaturization of the onboard data handling system of a small satellite.

A mixed-mode application-specific integrated circuit (ASIC) that represents a single chip implementation of an onboard command and data handling (OBCDH) subsystem for a low-cost small satellite was proposed.[2] The ASIC specification is based on requirements of future small satellites for Earth observation missions and therefore, in addition to data processing and control functions, it features enhanced remote sensing and data gathering capabilities. Figure 1 shows the block diagram of the SoC ASIC, which consists of four subsystems: a 32-bit RISC processor core modified for space use; an image handling subsystem capable of capturing and compressing still or video-rate images; a communication subsystem for the satellite uplink and downlink connection; and a supporting peripheral subsystem.

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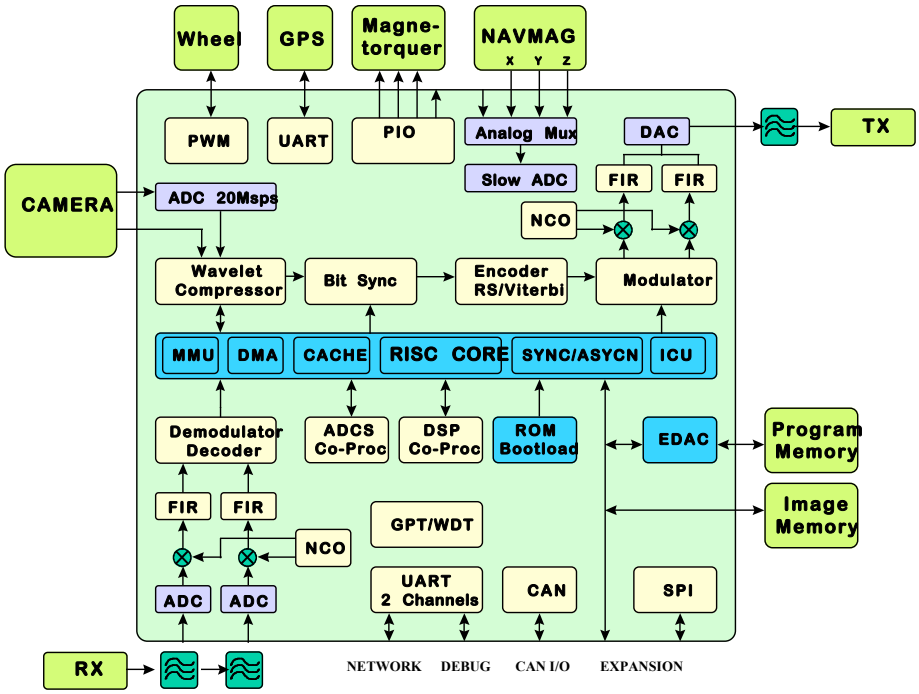

Fig. 1 OBCDH ASIC block-diagram.

Small satellite development is targeted at achieving affordable and fast access to space. While ideal in terms of density and reliability, a mixed-mode ASIC solution to a single chip OBCDH system is prohibitively expensive, being justified only in case of mass volume production. One financially viable implementation option is to use high-density field-programmable gate arrays (FPGA). FPGAs offer a number of advantages that are very relevant to the specifics of small satellite design: flexibility of design, shorter time-to-market, lower cost, remote reconfigurability, etc. So far, high-density FPGAs have been mostly used in payload systems of small satellites, however introduction of radiation hardened versions of such devices by leading manufacturers as XILINX and Actel pave the way for their use in main onboard electronic systems.

Our practical efforts in miniaturizing the OBCDH system have started with its most essential component–the onboard computer (OBC). This paper presents the results of research work aimed at shrinking down an existing OBC design, which is manufactured as a printed circuit board, to an equivalent SoC design implemented on a high-density XILINX Virtex FPGA. This onboard computer system-on-a-chip (SoC-OBC) can serve as an initial prototype of the digital part of the OBDH ASIC in Figure 1, or can be used on its own as an OBC implementation on a single programmable chip. Such a programmable SoC can be made further reconfigurable so that the design can be changed dynamically on board a satellite upon request.

The paper is structured as follows. The first section details the structure of the SoC-OBC and the adopted design approach. The second section outlines intellectual property (IP) core integration resulting in a downsized implementation of the SoC-OBC. The third section describes the structure, functions, and simulation of a software communication system for the SoC-OBC. The fourth section describes a mathematical co-processor IP core for the SoC-OBC. The last section briefly discusses reconfiguration aspects of the SoC-OBC.

II. Single Chip Onboard Computer—Specification and Design Approach

SoC design is much more than high-level integration of IP cores such as microprocessors, memory, and peripherals. It requires "application domain expertise" and "application domain know-how" in order to maximize the effect of translating system functionality to a single-chip implementation. In fact it is a common practice that customers participate in SoC design alongside manufacturers by undertaking requirements analysis and application specific IP core development. The SoC work reported here was conducted in close collaboration with Surrey Satellite Technology Ltd. (SSTL), who have successfully designed and manufactured micro- and mini- satellites for more than 20 years.

"SoC design is the next step in the technology evolution that represents the combined tools and methodology to effectively develop very large complex systems, on a single silicon substrate, in a very short design cycle. The integration side of SoC design starts with partitioning of the system around the primarily pre-existing, block-level functions and identifying the new or differentiating functions needed. SoC designs are typically either derivative designs with increased functionality, or convergence designs where previously separate functions are integrated."[*] In this project we were dealing with the latter—an existing primary onboard computer OBC386, developed by SSTL[†] and flown on several small satellite missions, was used as a reference design. The main goal was to translate the technical capabilities of the OBC to a single-chip design achieving a cost-effective solution. The straightforward approach to that would be to purchase commercially available IP cores compatible with the integrated circuits (IC) in the OBC circuit board and to integrate them onto a single chip. This approach was ruled out at the beginning, however, because it was realized that it would lead to a very expensive product. Also it appeared that a soft IP core of the 386EX microcontroller was not available. We then decided to go for an approach based on using public domain soft IP cores where possible as well as in-house peripheral IP core development. Two of the employed IP cores, the LEON microprocessor IP core and the HurriCANe controller area network (CAN) IP core, are developed by the European Space Agency (ESA). The LEON processor IP core includes support for the Advanced Microcontroller Bus Architecture (AMBA) protocol, and therefore the AMBA bus is selected as the on-chip bus for the SoC. The following CAD software packages were used during the development: VHDL simulator ModelSim, synthesis tool Synplify Pro and XILINX Integrated Software Environment (ISE).

Figure 2 shows the block-diagram of the SoC-OBC. It consists of a 32-bit SPARC V8 compliant microprocessor core, LEON,[3] connected via a system bus to a ROM bootstrap loader and a memory error-detection-and-correction (EDAC) unit, an AMBA AHB on-chip bus[‡] and a number of peripheral modules. The LEON microprocessor core can be downloaded from http://www.gaisler.com free of charge. The modules developed in-house are as follows: an EDAC unit, a bootstrap loader, an HDLC controller, a network interface, a true IDE interface, a floating-point Coordinate Rotation Digital Computer (CORDIC) mathematical co-processor and AMBA bus peripheral interface modules. The correspondence of the SoC-OBC to the reference OBC model is shown in Figure 3.

Results of a feasibility study provided estimates of the required area and performance of the LEON-based SoC-OBC, which showed that the XILINX Virtex family of SRAM-based FPGAs could serve as a suitable implementation medium.[4]

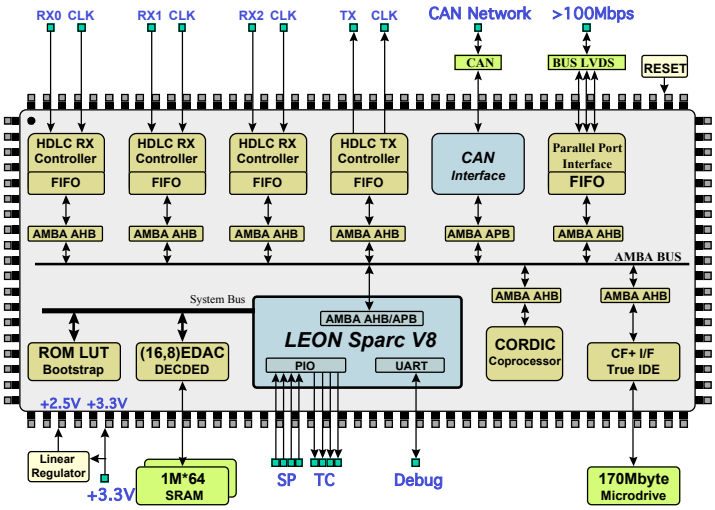

Fig. 2 SoC-OBC block-diagram.

[*]Linchpin Technologies and Methodologies for Change, White Paper, 1999, http://www.cadence.com/whitepapers/linchpin.pdf (cited Dec. 2003).
[†]OBC386 Datasheet, http://www.sstl.co.uk/services/subpage_services.html (cited Dec. 2003).
[‡]Data available online at http://www.arm.com/sitearchitek/armtech.ns4/html/amba (cited Dec. 2003).

III. Implementation of a Downsized SoC-OBC Prototype

A downsized version of the SoC-OBC was implemented on a XILINX Virtex XCV800 FPGA (HQ240, speed –4) using a XESS XSV-800 prototyping board.* The downsized system represents a main subsystem of the SoC-OBC and consists of the LEON processor, the HurriCANe core and an EDAC core. Figure 4 shows a diagrammatic representation of the integrated design and the experimental setup. As illustrated in Figure 4, the HurriCANe core is integrated with the LEON processor core through the AMBA Advanced Peripheral Bus (APB). An external CAN controller card is employed in addition to the XESS prototyping board to test the CAN core. The CAN IP core and the external CAN card act as two equivalent nodes on the CAN bus.

Three versions of the LEON IP core—LEON-1, ver. 2.2.2 and 2.4.0; and LEON-2, ver. 1.0.2a—were implemented and verified at 25 MHz on the XESS prototyping board. The implementation of the downsized SoC-OBC requires about half of the capacity of a XILINX Virtex XCV800 FPGA and the resultant bit-stream file measures 576 kB. The whole SoC-OBC, excluding the CORDIC co-processor, fits in about three quarters of a XILINX Virtex XCV800 chip.

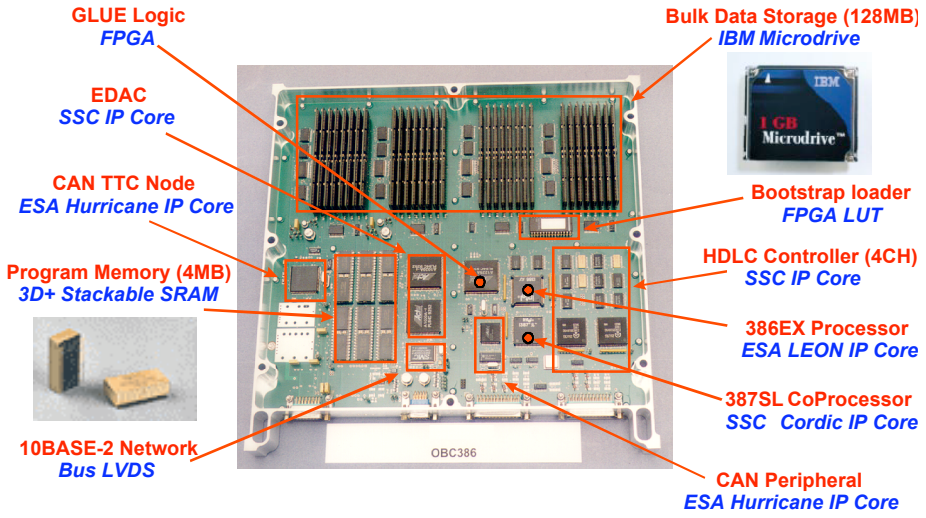

Fig. 3 Mapping of the OBC386 reference model.

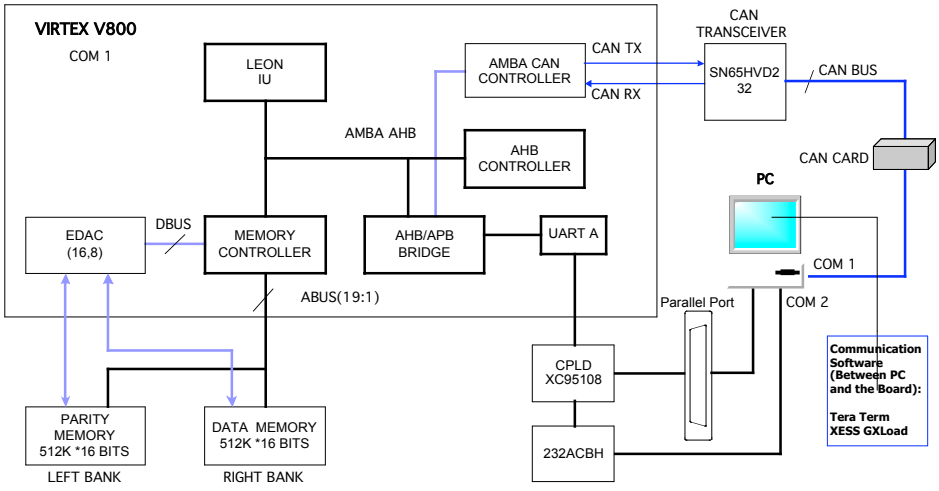

Fig. 4 Downsized SoC-OBC-integration and test.

* Data about the Virtex Prototyping Board XSV800 is available online at http://www.xess.com (cited Dec. 2003).

IV. Development of a Communication System for the SoC-OBC

An OBC should be able to accept telecommand (TC) data from the ground station and send back telemetry (TLM) data. A low-cost communication system was designed, which consisted of a software package implementing the data transmission protocol and a thin-layer hardware interface.[5] The software package is based on the Consultative Committee of Space Data Systems (CCSDS) protocol, which is a space industry communication standard for TC and TLM transmission, employed on numerous missions ranging from relatively simple low-Earth orbit missions to deep space probes.

The complete implementation of the CCSDS TLM and TC protocol is very complex and expensive. Therefore, the developed CCSDS software package focuses on a subset of functions such that it represents a simplified yet reliable stand-alone alternative software implementation of the CCSDS TLM and TC Command Operation Protocol, COP-1.

The CCSDS software package features a modular structure, which can facilitate easy expansions of functionality to suit specific mission requirements. The size of the CCSDS software is as follows: ground segment including the Reed-Solomon (R-S) decoder-177 kB; spacecraft segment including the R-S encoder-176 kB; R-S encoder/decoder-21.7 kB. The software imposes minimal memory footprint and performance requirements on the OBC.

The functionality of the communication system was verified with software TLM/TC loop using the downsized SoC-OBC implementation, described previously.[6] The onboard segment was executed on the SoC-OBC, and the ground station segment on a personal computer. Communication between the two segments was simulated via a serial link. A CAN bus system consisting of two nodes, the HurriCANe IP core and a CAN controller card, was used to close the data transmission loop. The CAN card emulated the responsibilities of an onboard payload which generates TLM data and receives TC data.

Figure 5 shows the simulation data-flow. Simulation scenarios covering the entire communication data-flow cycle—sending of TC data to the spacecraft; onboard processing of TC data; generation and sending of TLM data to ground—were tested successfully. The simulation results proved that all the main blocks of the communication system worked according to specification and that the SoC-OBC correctly executed the functions of the onboard segment. The combination of an OBC implemented on a single FPGA and a CCSDS-based software communication system could provide a cost effective and flexible communication solution for miniaturized small satellites.

V. Mathematical CORDIC Co-Processor IP Core

Data processing on board small satellites is becoming more sophisticated and therefore there is an increased need for fast calculation of computationally intensive mathematical routines. One example of such processing is the execution of attitude control and determination system (ADCS) algorithms. This section gives details of the mathematical co-processor IP core of the SoC-OBC in Figure 2. The co-processor IP core is based on the CORDIC algorithm[7] and is capable of computing 17 mathematical functions: sine, cosine, tangent, inverse sine, inverse cosine, inverse tangent, hyperbolic sine, hyperbolic cosine, hyperbolic tangent, inverse hyperbolic tangent, exponential, square root, natural log, addition, subtraction, multiplication, and division. The co-processor conforms to the IEEE-754 standard for single-precision (32-bit) floating-point numbers, handling overflow, underflow, and special number representations, such as infinity and "not-a-number".[8]

A register-transfer level (RTL) specification of the co-processor was captured in the hardware description language VHDL. Before any VHDL work was carried out, however, the floating-point operation of the CORDIC algorithm was fully investigated via software modeling at bit-level. Extensive testing of the numerical results, generated by the co-processor, verified correctness and showed a good level of accuracy. The RTL design was fully tested and debugged, leading to the final version of the VHDL code, which was then synthesized and implemented on a XILINX Virtex XCV800 chip. The co-processor was then integrated with the LEON-2 microprocessor IP core (ver. 1.0.9) and its operation was tested on a XILINX Virtex XCV800 FPGA using the XESS XSV800 prototyping board as shown in Figure 6. The co-processor showed good performance speeding up the execution of the Whetstone benchmark 1.8 times. The co-processor IP core occupies half of the area of a Virtex XCV800 chip.

VI. Reconfiguration Aspects

Small satellite electronic components are generally unavailable for physical upgrade or repair after launch. This restriction could be overcome by uploading representations of hardware circuits via a radio link. Run-time reconfiguration of SRAM-based FPGAs provides a solution to introducing changes in the implemented design dynamically, i.e. without interrupting its operation.

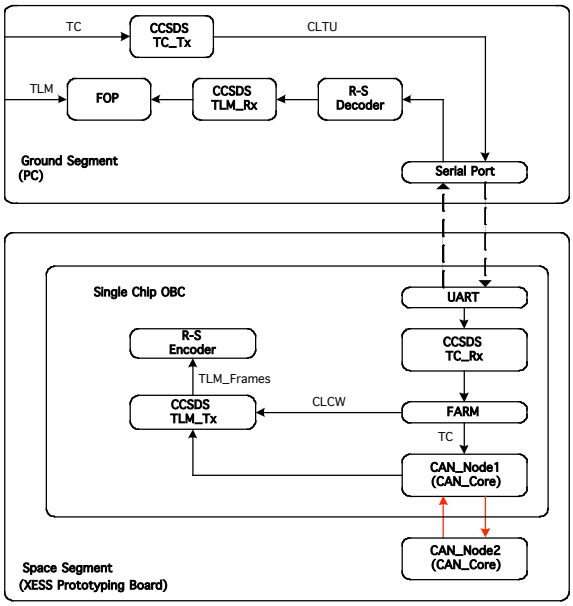

Fig. 5 Simulation data flow of the CCSDS communication system.

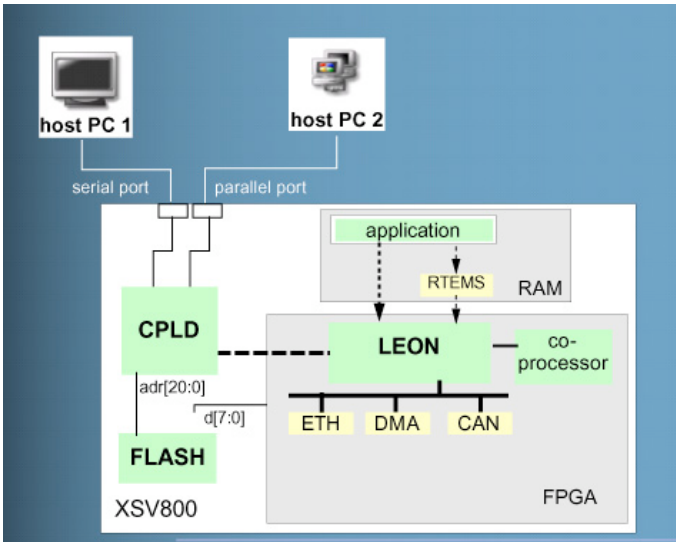

Fig. 6 Integration of the co-processor IP core with LEON.

Because the XILINX Virtex series of FPGAs support run-time partial reconfiguration, a SoC-OBC implementation using that platform could be made dynamically reconfigurable. The presence of a run-time reconfiguration capability would allow OBCDH designers to change the functionality of the SoC-OBC remotely. For example, application specific peripheral IP cores can be upgraded and replaced, or new ones can be added. A mechanism for remote reconfiguration of the SoC-OBC is in development.[9] A client-server scheme, which uses XILINX Virtex FPGAs and run-time reconfiguration technology, is illustrated in Figure 7. This scheme is based on the XILINX hardware interface (XHWIF) and the use of Internet (TCP/IP) protocols for communication between spacecraft and the ground. The run-time partial reconfiguration of the Virtex based SoC-OBC is achieved by using the XILINX development environment JBits and integrating it with the XHWIF interface.

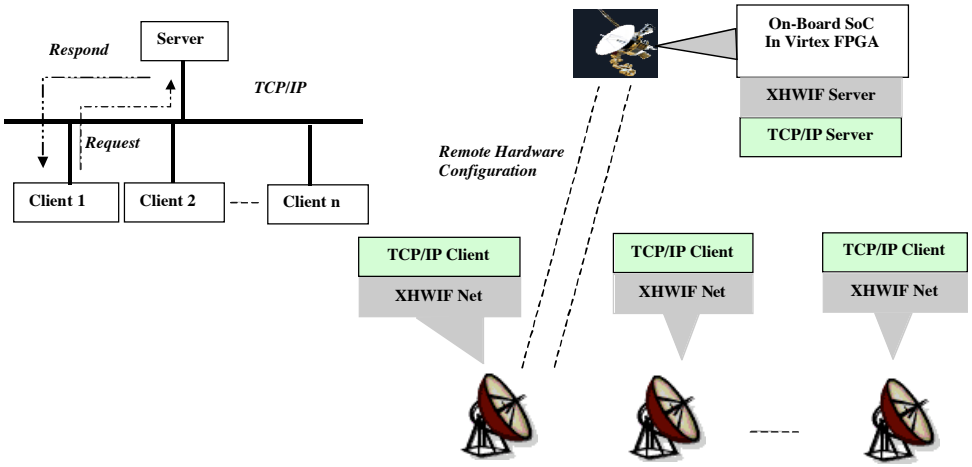

Fig. 7 Onboard SoC run-time reconfiguration – client server scheme.

VII. Conclusions

As a result of their low cost, flexibility, and increased density, programmable logic chips could replace ASICs as an implementation medium for OBCDH SoC development. This paper presents a novel FPGA implemented design for an onboard computer SoC intended for a low-cost small satellite. The functionality of an existing onboard computer was mapped onto a SoC that was designed using soft reusable IP cores. Area and performance estimates indicate that the entire SoC-OBC design can be implemented on a single FPGA chip with capacity not exceeding that of a XILINX Virtex XCV2000E chip. Application of reconfigurable technology to the SoC-OBC could lead to a new generation of upgradeable and hence evolvable OBCs.

Development of main components of the SoC-OBC was successfully attempted as follows. A downsized version of the SoC-OBC, consisting of the LEON, CAN, and EDAC IP cores, was implemented on a XILINX Virtex XCV800 chip. A low-cost communication system based on the CCSDS protocol was developed and simulated. A mathematical co-processor IP core, based on the CORDIC algorithm, was developed and integrated with the LEON-2 microprocessor core. Testing results showed that the co-processor significantly speeded up execution of floating point calculations.

"In designing electronic and computer systems for space applications we aim to optimize the availability, capability, flexibility and reliability of the system while minimizing cost and risk."[10] Technological advances, such as system-on-a-chip design, reusable IP core techniques, and reconfigurable computing could assist spacecraft engineers in achieving that complex design goal and could lead to the development of miniaturized spacecraft with new capabilities.

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Special thanks are due to Jiri Gailer for creating and maintaining the open-source LEON processor IP core and its development environment, which is a great asset to the SoC design community and serves as a driving force for many exciting SoC projects worldwide.

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